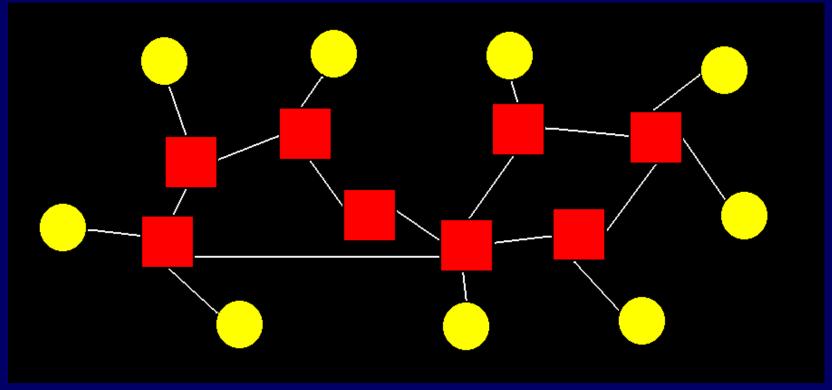
ACTIVE Interconnects Let's have some guts!

Jonathan M. Smith (with I. Hadzic and W. Marcus) http://www.cis.upenn.edu/~jms

Current IP Networking Religion:

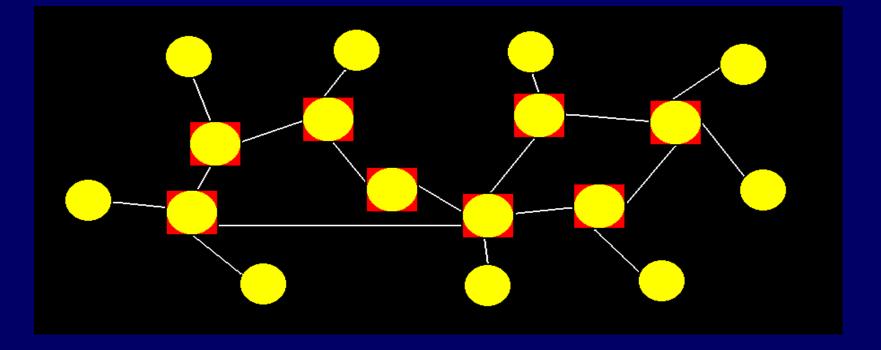
Smart hosts on the edges
Dumb switches in the center



Active Networking

Can change network behavior on-the-fly

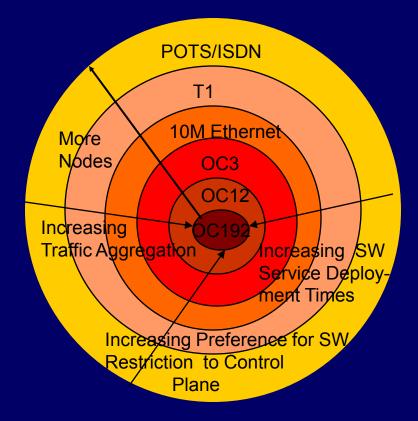
- In-band capsules
- Out-of-band loadable modules
- Details? See http://www.cis.upenn.edu/~switchware



Applications and Challenges

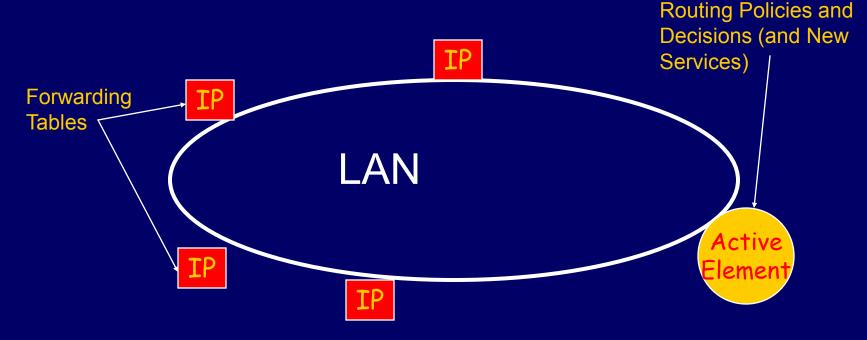
 Allow user customization of network
 E.g., caching, routing, transcoding, etc.
 Concerns: Flexibility, Usability, Security and PERFORMANCE
 For example, is Active Networking even relevant in an all-optical network?

Activation potential at various commercially deployed rates:



Solution: Active Router Control (stay out of forwarding path)

IP Router/Forwarders co-located with Active Elements:

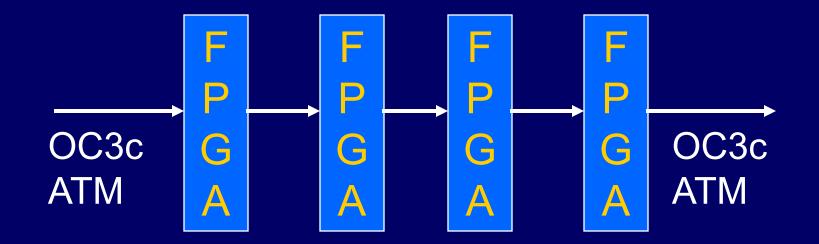


Can we do more? Or do optics invalidate Active Nets vision?

Approach:

look at the other exponential technologies
processor clock rates track bandwidths
exotic technologies, e.g., mediaprocessors
general-purpose CPUs? Maybe.....

Protocol Processing Pipeline (P4)

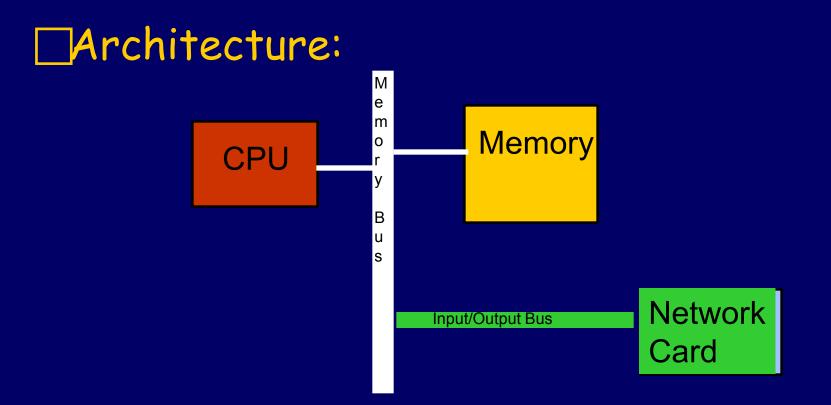


http://www.cis.upenn.edu/~boosters

Some rough arithmetic...

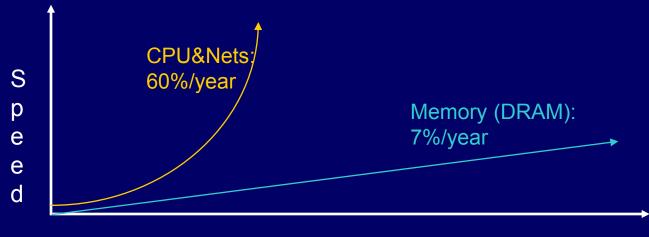
 \Box OC192c SONET is 9.6 Gb/s For 64 bit CPU, 150 MW/s Clock rates of 500-750 MHz mean: **RR** moves: 2-3 W/instruction Register file writes likely bottleneck So about 5 instructions/word Can't afford any delays

Typical Computing, Memory & Network Attachment



Why this won't work: mismatched exponentials

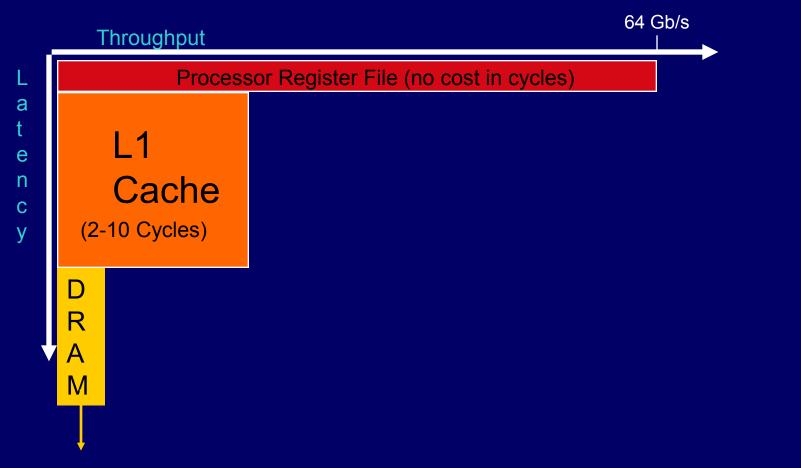
Memory exponential has been <u>capacity</u>



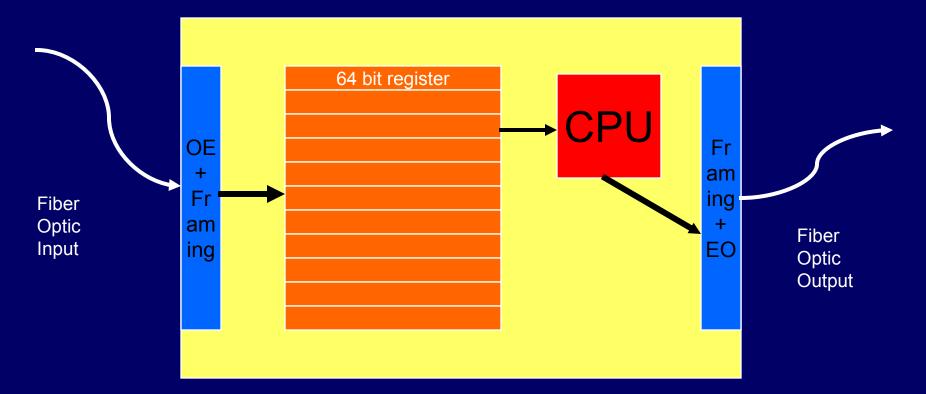
Calendar Time

Not throughput!

Unattractive tradeoffs for networks:



Fiber-coupled processing?



Register-Only Media Processor (ROMP)

Summary

Many attractions of active networking
Can trade away flexibility for performance
Can get out of the fast path (ARC), or
Specialized HW in fast path: The P4, or
Glue a CPU in the fast path (ROMP)
http://www.cis.upenn.edu/~switchware